

## 56.1 TEST—Logical Compare

Opcode	Instruction	Description
A8 <i>ib</i>	TEST AL, <i>imm8</i>	AND <i>imm8</i> with AL; set SF, ZF, PF according to result
A9 <i>iw</i>	TEST AX, <i>imm16</i>	AND <i>imm16</i> with AX; set SF, ZF, PF according to result
A9 <i>id</i>	TEST EAX, <i>imm32</i>	AND <i>imm32</i> with EAX; set SF, ZF, PF according to result
F6 /0 <i>ib</i>	TEST <i>r/m8</i> , <i>imm8</i>	AND <i>imm8</i> with <i>r/m8</i> ; set SF, ZF, PF according to result
F7 /0 <i>iw</i>	TEST <i>r/m16</i> , <i>imm16</i>	AND <i>imm16</i> with <i>r/m16</i> ; set SF, ZF, PF according to result
F7 /0 <i>id</i>	TEST <i>r/m32</i> , <i>imm32</i>	AND <i>imm32</i> with <i>r/m32</i> ; set SF, ZF, PF according to result
84 /r	TEST <i>r/m8</i> , <i>r8</i>	AND <i>r8</i> with <i>r/m8</i> ; set SF, ZF, PF according to result
85 /r	TEST <i>r/m16</i> , <i>r16</i>	AND <i>r16</i> with <i>r/m16</i> ; set SF, ZF, PF according to result
85 /r	TEST <i>r/m32</i> , <i>r32</i>	AND <i>r32</i> with <i>r/m32</i> ; set SF, ZF, PF according to result

### Description

Computes the bit-wise logical AND of first operand (source 1 operand) and the second operand (source 2 operand) and sets the SF, ZF, and PF status flags according to the result. The result is then discarded.

### Operation

```
TEMP ← SRC1 AND SRC2;
SF ← MSB(TEMP);
IF TEMP = 0
    THEN ZF ← 0;
    ELSE ZF ← 1;
FI:
PF ← BitwiseXNOR(TEMP[0:7]);
CF ← 0;
OF ← 0;
(*AF is Undefined*)
```

### Flags Affected

The OF and CF flags are cleared to 0. The SF, ZF, and PF flags are set according to the result (see the “Operation” section above). The state of the AF flag is undefined.

### Protected Mode Exceptions

#GP(0)	If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
	If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)	If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)	If a page fault occurs.
#AC(0)	If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

### Real-Address Mode Exceptions

- |     |   |
|-----|---|
| #GP | If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit. |
| #SS | If a memory operand effective address is outside the SS segment limit.                    |

### Virtual-8086 Mode Exceptions

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|-----------------|---|
| #GP(0)          | If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit. |
| #SS(0)          | If a memory operand effective address is outside the SS segment limit.                    |
| #PF(fault-code) | If a page fault occurs.   |
| #AC(0)          | If alignment checking is enabled and an unaligned memory reference is made.               |